(9) Kindly add Claim 22 as follows:

--22. (New Claim) The method as recited in Claim 9 wherein the sidewall spacer is not formed contiguous the side of the channel region.--

REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-20 in the application. Presently, the Applicants have amended Claims 1, 5-6, 9, 13-14 and 17 and have added Claims 21 and 22. Currently, no claims have been canceled. Accordingly, Claims 1-22 are currently pending in the application.

I. Rejection of Claims 1, 2, 5, 7, 9, 10, 13, 15 and 17-20 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 5, 7, 9, 10, 13, 15 and 17-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,834,793 to Shibata (Shibata). Presently, the Applicants have amended Claims 1, 9 and 17 to include the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region. Support for this amendment can be found at paragraph 46 of the application as filed. Further support for this amendment may be found in FIGUREs 1A-1B and 9-20. The Applicants assert that Shibata fails to teach the newly amended element.

Shibata is directed to a semiconductor device using resonant tunneling. (Column 1, lines 65-66). Shibata teaches a structure that has a SiO_2 buried layer 305 positioned along a sidewall

contiguous with the channel region 306. Shibata also teaches that the SiO_2 buried layer 305 has a thickness that is small enough to allow a flow of direct tunneling current when a voltage difference is applied between the source 302 and drain 302'. (Column 3, lines 15-40).

While Shibata may teach a SiO_2 buried layer 305 positioned along a sidewall contiguous with the channel region 306, it does not teach forming a sidewall spacer over at least one sidewall of the trench distal the channel region. Specifically, the only sidewall spacer which might have been taught by Shibata (i.e., the SiO_2 buried layer 305) is located contiguous with the channel region and not distal the channel region.

Therefore, Shibata does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 2, 5, 7, 10, 13, 15 and 18-20 are dependent upon Claims 1, 9 and 17, Shibata also cannot be an anticipating reference for Claims 2, 5, 7, 10, 13, 15 and 18-20. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

II. Rejection of Claims 1, 3, 9 and 11 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 3, 9 and 11 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,346,729 B1 to Liang, *et al.* (Liang). As previously recited, the Applicants have amended Claims 1, 9 and 17 to include the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region. The Applicants assert that Liang fails to teach the newly amended element.

Liang is directed to a process for forming a MOSFET device, featuring a heavily doped source/drain region isolated from a semiconductor substrate, via the use of a thin silicon oxide layer. (Abstract) Liang teaches that its silicon dioxide layers 9 and 9' are positioned in a base of its trench

8a and along a sidewall contiguous with the channel region. More specifically, independent Claim 1 of Liang requires that "an L shaped, thin silicon oxide layer, comprised of a vertical shape, extending vertically downward from the bottom of said lightly doped source/drain segment [i.e., contiguous with the channel region] and a horizontal shape, extending horizontally from the bottom of said vertical shape of said L shaped thin silicon oxide layer, to the side of an insulator filled shallow trench isolation region." (Claim 1--Emphasis added)

While Liang may teach silicon dioxide layers 9 and 9' positioned in a base of its trench 8a and along a sidewall contiguous with the channel region, it does not teach forming a sidewall spacer over at least one sidewall of the trench distal the channel region.

Therefore, Liang does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 3 and 11 are dependent upon Claims 1 and 9, Shibata also cannot be an anticipating reference for Claims 3 and 11. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

III. Rejection of Claims 4 and 12 under 35 U.S.C. §103

The Examiner has rejected Claims 4 and 12 under 35 U.S.C. §103(a) as being unpatentable over Shibata as applied to Claims 1 and 9 above, and further in view of U.S. Patent No. 6,344,669 B1 to Pan (Pan). As established above, Shibata fails to teach every element recited in independent Claims 1, 9 and 17, and more specifically, those elements newly amended into such claims.

Additionally, Shibata fails to suggest such elements. Shibata fails to suggest such an element because Shibata is only focused on placing its SiO_2 buried layer 305 between its source/drain regions 302, 302' to allow or prevent resonant tunneling between its source/drain

regions 302, 302' and the channel region 306. Further, there is no motivation in the teachings or suggestions of Shibata to move its SiO_2 buried layer 305 to a distal sidewall, as required by the claimed invention, because to do so would render the SiO_2 buried layer 305 useless for its intended purpose.

Similarly, Pan fails to teach or suggest the newly amended element. The Examiner is using Pan for the sole proposition that the source/drain regions may be formed of epitaxial silicon. Notwithstanding the merits of the Examiner's position, Pan also fails to teach or suggest the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region. A teaching or suggestion of using epitaxial silicon for the source/drain regions is dissimilar to a teaching that a sidewall spacer be located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17.

Accordingly, the combination of Shibata and Pan fails to teach or suggest the invention recited in independent Claims 1, 9 and 17 and their dependent claims, when considered as a whole. Thus, the combination has failed to establish a prima facie case of obviousness with respect to Claims 1, 9 and 17 and their dependent claims. Claims 4 and 12 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 4 and 12 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

IV. Rejection of Claims 6 and 14 under 35 U.S.C. §103

The Examiner has rejected Claims 6 and 14 under 35 U.S.C. §103(a) as being unpatentable over Shibata. The Applicants established in the §103 rejection above that Shibata fails to teach or suggest the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17. Accordingly, Shibata has failed to establish a prima facie case of obviousness with respect to Claims 1, 9 and 17 and their dependent claims. Claims 6 and 14 are therefore not obvious in view of Shibata.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 6 and 14 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

V. Rejection of Claims 8 and 16 under 35 U.S.C. §103

The Examiner has rejected Claims 8 and 16 under 35 U.S.C. §103(a) as being unpatentable over Shibata in view of Liang. The Applicants established in the §103 rejection above that Shibata fails to teach or suggest the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17. The Applicants also established in a §102 rejection above that Liang fails to teach such an element.

Similar to Shibata, Liang fails to suggest the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region. Liang fails to suggest such an element because Liang uses its shallow trench isolation structures 2 to provide its isolation distal the channel region, and therefore would not require a sidewall spacer be located there also. One skilled in the art would not be motivated to take the thin silicon dioxide layers 9, 9b taught by Liang and place

it on the sidewall distal the channel without using the present invention as a blueprint. Thus, Liang also fails to teach or suggest such an element.

Accordingly, the combination of Shibata and Liang fails to teach or suggest the invention recited in independent Claims 1, 9 and 17 and their dependent claims, when considered as a whole. Thus, the combination has failed to establish a prima facie case of obviousness with respect to Claims 1, 9 and 17 and their dependent claims. Claims 8 and 16 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 8 and 16 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

VI. Rejection of Claims 8 and 16 under 35 U.S.C. §103

The Examiner has rejected Claims 8 and 16 under 35 U.S.C. §103(a) as being unpatentable over Liang. For the same reasons that the combination of Shibata and Liang fails to teach or suggest every element recited in independent Claims 1, 9 and 17 of the present invention, Liang alone fails to teach or suggest every element recited in independent Claims 1, 9 and 17 of the present invention.

Accordingly, Liang fails to teach or suggest the invention recited in independent Claims 1, 9 and 17 and their dependent claims, when considered as a whole. Thus, Liang has failed to establish a prima facie case of obviousness with respect to Claims 1, 9 and 17 and their dependent claims. Claims 8 and 16 are therefore not obvious in view of the combination.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 8 and 16 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

VII. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-22.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Kindly rewrite Claim 1 as follows:

1. (Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region; and

a source/drain region located over the isolation structure.

(2) Kindly rewrite Claim 5 as follows:

5. (Amended) The semiconductor device as recited in Claim 1 wherein [a side wall of the trench includes] an oxide layer is located between the sidewall spacer and the at least one sidewall of the trench.

(3) Kindly rewrite Claim 6 as follows:

6. (Amended) The semiconductor device as recited in Claim [5 further including a nitrided layer located on the oxide layer] 1 wherein the sidewall spacer comprises a nitrided layer.

(4) Kindly rewrite Claim 9 as follows:

9. (Amended) A method of manufacturing a semiconductor device, comprising:

forming a channel region in a semiconductor substrate;

forming a trench adjacent a side of the channel region;

forming an isolation structure in the trench;

forming a sidewall spacer over at least one sidewall of the trench distal the channel region; and

forming a source/drain region over the isolation structure.

(5) Kindly rewrite Claim 13 as follows:

13. (Amended) The method as recited in Claim 9 further including forming an oxide layer [on a side wall of the trench] between the sidewall spacer and the at least one sidewall of the trench.

(6) Kindly rewrite Claim 14 as follows:

14. (Amended) The method as recited in Claim [13 further including forming a nitrided layer on the oxide layer] wherein forming a sidewall spacer includes forming a nitrided layer.

(7) Kindly rewrite Claim 17 as follows:

17. (Amended) An integrated circuit, comprising:

semiconductor devices, including;

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region; and

a source/drain region located over the isolation structure; and

dielectric layers located over the semiconductor devices and having interconnect structures located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

(8) Kindly add Claim 21 as follows:

--21. (New Claim) The semiconductor device as recited in Claim 1 wherein the sidewall spacer is not contiguous the side of the channel region.--

(9) Kindly add Claim 22 as follows:

--22. (New Claim) The method as recited in Claim 9 wherein the sidewall spacer is not formed contiguous the side of the channel region.--